CLAIMS

1. A transistor comprising:

a source (a "ferromagnetic source") that is made of a ferromagnetic material and injects carriers;

a drain that receives the carriers injected from the ferromagnetic source;

a tunnel barrier (a "ferromagnetic tunnel barrier") that is located between the ferromagnetic source and the drain and is made of a ferromagnetic material; and

a gate electrode that is formed in relation to the ferromagnetic tunnel barrier, and controls carrier conduction from the ferromagnetic source to the drain by inducing an electric field in the ferromagnetic tunnel barrier,

the energy band edge of the conduction band in the ferromagnetic tunnel barrier being spin-split when the carriers are electrons,

the energy band edge of the valence band in the ferromagnetic tunnel barrier being spin-split when the carriers are holes.

2. The transistor as claimed in claim 1, further comprising

a gate insulating film that is formed between the ferromagnetic tunnel barrier and the gate electrode.

3. The transistor as claimed in claim 1 or 2, wherein:

the ferromagnetic tunnel barrier exhibits a low tunnel barrier to the major-spin electrons in the ferromagnetic source when the magnetization direction of the ferromagnetic tunnel barrier is the same as the magnetization direction of the ferromagnetic source or the direction of the major spin in the ferromagnetic source is the same as the spin direction of the spin

band at the energy band edge of the ferromagnetic tunnel barrier (the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier being "parallel magnetization"); and

the ferromagnetic tunnel barrier exhibits a high tunnel barrier to the major-spin electrons in the ferromagnetic source when the magnetization direction of the ferromagnetic tunnel barrier is opposite to the magnetization direction of the ferromagnetic source or the direction of the major spin in the ferromagnetic source is different from the spin direction of the spin band at the energy band edge of the ferromagnetic tunnel barrier (the relative magnetization direction being "parallel magnetization").

4. The transistor as claimed in claim 1 or 2, wherein the ferromagnetic tunnel barrier has a tunnel probability that can be controlled in relation to the major spin in the ferromagnetic source, in accordance with a voltage to be applied to the gate electrode (the voltage being "gate voltage"), when the ferromagnetic source and the ferromagnetic tunnel barrier exhibit the parallel magnetization.

5. The transistor as claimed in claim 1 or 2, wherein the ferromagnetic tunnel barrier has such a thickness that the major spin in the ferromagnetic source tunneling the ferromagnetic tunnel barrier generates a current through application of a gate voltage to the ferromagnetic tunnel barrier, when the ferromagnetic source and the ferromagnetic tunnel barrier exhibit the parallel magnetization.

6. The transistor as claimed in claim 1 or 2, wherein a threshold voltage is set as such a gate voltage as to generate a predetermined current between the ferromagnetic source and the drain through

application of a gate voltage, when the ferromagnetic source and the ferromagnetic tunnel barrier exhibit the parallel magnetization.

7. The transistor as claimed in claim 1 or 2, wherein, when the ferromagnetic source and the ferromagnetic tunnel barrier exhibit the antiparallel magnetization, a current generated between the ferromagnetic source and the ferromagnetic drain is lower than a current caused in the case of the parallel magnetization, the current in the case of the antiparallel magnetization being caused because the barrier height of the ferromagnetic tunnel barrier in relation to the major-spin electrons in the ferromagnetic source is higher by the width of a spin split caused at the energy band edge.

8. The transistor as claimed in claim 1 or 2, wherein mutual conductance can be controlled in accordance with the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier, with the same bias being applied.

9. The transistor as claimed in any of claims 1 to 8, wherein the source is made of a half-metal ferromagnetic material, or the source and the drain are made of a half-metal ferromagnetic material.

10. The transistor as claimed in any of claims 1 to 9, further comprising a non-magnetic member between the ferromagnetic source and the ferromagnetic tunnel barrier.

11. The transistor as claimed in any of claims 1 to 8 and 10, wherein the drain is either a non-magnetic member or a ferromagnetic member.

12. A transistor comprising:

a non-magnetic source that is made of a non-magnetic material and injects carriers;

a ferromagnetic drain that receives the carriers injected from the non-magnetic source;

a ferromagnetic tunnel barrier that is located between the non-magnetic source and the ferromagnetic drain and is made of a ferromagnetic material; and

a gate electrode that is formed in relation to the ferromagnetic tunnel barrier, and controls carrier conduction from the non-magnetic source to the ferromagnetic drain by inducing an electric field in the ferromagnetic tunnel barrier,

the energy band edge of the conduction band in the ferromagnetic tunnel barrier being spin-split when the carriers are electrons,

the energy band edge of the valence band in the ferromagnetic tunnel barrier being spin-split when the carriers are holes.

13. A transistor comprising:

a substrate;

a junction structure that is formed on the substrate, and comprises a ferromagnetic source that injects carriers, a drain that receives the carriers injected from the ferromagnetic source, and a ferromagnetic tunnel barrier that is located between the ferromagnetic source and the drain; and

a gate electrode that controls carrier conduction from the ferromagnetic source to the drain by inducing an electric field in the ferromagnetic tunnel barrier,

the energy band edge at the bottom of the conduction band in the ferromagnetic tunnel barrier being spin-split when the carriers are electrons,

the energy band edge at the top of the valence band in the ferromagnetic tunnel barrier being spin-split when the carriers are holes,

the junction structure having a joined surface in substantially the same direction as the normal direction of the substrate.

14. The transistor as claimed in claim 13, wherein the gate insulating film is formed on an exposed portion of the joined surface of the junction structure.

15. A transistor comprising:

a substrate;

a junction structure that is formed on the substrate, and comprises a ferromagnetic source that injects carriers, a drain that receives the carriers injected from the ferromagnetic source, and a ferromagnetic tunnel barrier that is located between the ferromagnetic source and the drain; and

a gate electrode that controls carrier conduction from the ferromagnetic source to the drain by inducing an electric field in the ferromagnetic tunnel barrier,

the energy band edge at the bottom of the conduction band in the ferromagnetic tunnel barrier being spin-split when the carriers are electrons,

the energy band edge at the top of the valence band in the ferromagnetic tunnel barrier being spin-split when the carriers are holes,

the junction structure having a joined surface in substantially the same direction as a direction parallel to the substrate.

16. The transistor as claimed in claim 15, wherein the gate insulating film is formed on an exposed portion of the joined surface of the junction structure.

17. A memory element comprising:

a transistor as claimed in any of claims 1 to 16,

the memory element storing information in accordance with the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier,

the memory element detecting information stored in the transistor in accordance with output characteristics based on the mutual conductance of the transistor, the mutual conductance depending on the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier.

18. A memory element comprising:

a transistor as claimed in any of claims 1 to 16;

a first line that grounds the ferromagnetic source;

a second line that is connected to the drain; and

a third line that is connected to the gate electrode.

19. A memory element comprising:

a transistor as claimed in any of claims 1 to 16;

a first line that grounds the ferromagnetic source;

a second line that is connected to the drain;

a third line that is connected to the gate electrode; and

a fourth line that is connected to an output terminal that is formed at one end of the second line, and to a power source via a load, the fourth line branching out from the second line.

20. The memory element as claimed in claim 18 or 19, further comprising

a first extra line and a second extra line that cross each other on the transistor, while being electrically insulated from each other.

21. The memory element as claimed in claim 20, wherein the first extra line and the second extra line are replaced with the second line and the third line, or one of the first extra line and the second extra line is replaced with one of the second line and the third line.

22. The memory element as claimed in claim 20 or 21, wherein the memory element rewrites information by converting the magnetization of the ferromagnetic source or the ferromagnetic tunnel barrier to change the relative magnetization configuration of the ferromagnetic tunnel barrier with respect to the ferromagnetic source, using a magnetic field that is induced by flowing currents to the first extra line and the second extra line, or to the second line and the third line replacing the first extra line and the second extra line, or to one of the second line and the third line replacing one of the first extra line and the second extra line, and one of the first extra line and the second extra line that is not replaced.

23. The memory element as claimed in claim 20 or 21, wherein the memory element reads out information, based on the output characteristics of the transistor, the output characteristics being obtained by applying a first bias to the third line and applying a second bias between the first line and the second line.

24. The memory element as claimed in any of claims 19 to 23, wherein the memory device read out information in accordance with an output voltage that is obtained based on a voltage decrease in the load due to a current via the load and the transistor, the current being generated between the power source and the first line, when the first bias is applied to the

third line.

25. A memory circuit comprising:

transistors as claimed in any of claims 1 to 16, the transistors being arranged in a matrix fashion;

first lines that ground the ferromagnetic sources of the transistors independently of one another;

a plurality of word lines that are collectively connected to the gate electrodes of the transistors that are aligned in a column direction; and

a plurality of bit lines that are collectively connected to the ferromagnetic drains of the transistors that are arranged in a row direction.

26. A memory circuit comprising:

transistors as claimed in any of claims 1 to 16, the transistors being arranged in a matrix fashion;

first lines that grounds the ferromagnetic sources of the transistors independently of one another;

a plurality of word lines that are collectively connected to the gate electrodes of the transistors that are aligned in a column direction;

a plurality of bit lines that are collectively connected to the drains of the transistors that are aligned in a row direction;

output terminals each formed at one end of each corresponding one of the bit lines; and

second lines that branch out from the bit lines and are connected to a power source via a load.

27. The memory circuit as claimed in claim 25 or 26, further comprising

first extra lines and second extra lines that cross each other on the transistors, while being insulated from each other.

28. The memory circuit as claimed in claim 27, wherein the first extra lines and the second extra lines are replaced with the word lines and the bit lines, or either the first extra lines or the second extra lines are replaced with either the word lines or the bit lines.

29. The memory circuit as claimed in claim 27 or 28, wherein information is rewritten by converting the magnetization of the ferromagnetic source or the ferromagnetic tunnel barrier to change the relative magnetization configuration of the ferromagnetic tunnel barrier with respect to the ferromagnetic source, using a magnetic field that is induced by flowing currents to the first extra line and the second extra line, or to the second line and the third line replacing the first extra line and the second extra line, or to one of the second line and the third line replacing one of the first extra line and the second extra line, and one of the first extra line and the second extra line that is not replaced.

30. The memory circuit as claimed in claim 25 or 26, wherein information is read out based on the output characteristics of the transistor, the output characteristics being obtained by applying a first bias to the word line and applying a second bias between the first line and the bit line.

31. The memory circuit as claimed in any of claims 26 to 29, wherein information is read out in accordance with an output voltage that is obtained based on a voltage decrease in the load due to a current via the load and the transistor, the current being generated between the power source and the first line, when the first bias is applied to the word line.

32. A memory device comprising:

a first transistor and a second transistor as claimed in any of claims 1 to 16;

a first line that grounds a ferromagnetic source shared between the first and second transistors;

a second line and a third line that are connect to the drain of the first transistor and the drain of the second transistor; and

a fourth line that is connected to the gate electrode of the first transistor and the gate electrode of the second transistor.

33. A memory circuit comprising:

transistors as claimed in any of claims 1 to 11, 15, and 16, the transistors being arranged in a matrix fashion, the ferromagnetic sources of the transistors being collectively connected to the substrates or contact layers formed on the sides of the substrates and being grounded;

bit lines that are collectively connected to the drains of the transistors that are aligned in a row direction; and

word lines that are collectively connected to the gate electrodes of the transistors that are aligned in a column direction.

34. A two-terminal magnetoresistive element comprising:

a ferromagnetic source that injects carriers;

a drain that receives the carriers injected from the ferromagnetic source; and

a ferromagnetic tunnel barrier that is located between the ferromagnetic source and the drain,

the energy band edge of the conduction band in the ferromagnetic tunnel barrier being spin-split when the carriers are electrons,

the energy band edge of the valence band in the

ferromagnetic tunnel barrier being spin-split when the conduction carriers are holes.

35. A transistor comprising:

a ferromagnetic semiconductor layer;

a source that injects carriers into the ferromagnetic semiconductor layer;

a drain that receives the carriers injected into the ferromagnetic semiconductor layer; and

a gate electrode that applies a voltage for controlling conduction of the carriers from the source to the drain.

36. The transistor as claimed in claim 35, wherein one of the source and the drain is a ferromagnetic source or a ferromagnetic drain that comprises a tunnel barrier (a "non-magnetic tunnel barrier") that is made of a non-magnetic material and is joined to the ferromagnetic semiconductor layer, and an electrode (a "ferromagnetic electrode") that is made of a ferromagnetic material and is joined to the non-magnetic tunnel barrier.

37. The transistor as claimed in claim 35 or 36, wherein, when the source is the ferromagnetic source, the drain is a non-magnetic drain that comprises a non-magnetic tunnel barrier joined to the ferromagnetic semiconductor layer, and an electrode (a "non-magnetic electrode") that is made of a non-magnetic material and is joined to the non-magnetic tunnel barrier.

38. The transistor as claimed in claim 35 or 36, wherein, when the drain is the ferromagnetic drain, the source is a non-magnetic source that comprises a non-magnetic tunnel barrier joined to the ferromagnetic semiconductor layer, and a non-magnetic electrode joined to the non-magnetic tunnel barrier.

39. The transistor as claimed in claim 35, wherein the source and the drain each comprise a non-magnetic tunnel barrier joined to the ferromagnetic semiconductor layer, and a ferromagnetic electrode joined to the non-magnetic tunnel barrier.

40. The transistor as claimed in any of claims 35 to 39, wherein the non-magnetic tunnel barrier is made of a semiconductor that is the base material of the ferromagnetic semiconductor layer.

41. The transistor as claimed in claim 35, wherein one of the source and the drain is a ferromagnetic source or a ferromagnetic drain that comprises a tunnel barrier (a "ferromagnetic tunnel barrier") that is made of a ferromagnetic material and is joined to the ferromagnetic semiconductor layer, and a non-magnetic electrode joined to the ferromagnetic tunnel barrier.

42. The transistor as claimed in claim 35 or 41, wherein, when the source is the ferromagnetic source, the drain is a non-magnetic drain that comprises a non-magnetic tunnel barrier joined to the ferromagnetic semiconductor layer, and a non-magnetic electrode joined to the non-magnetic tunnel barrier.

43. The transistor as claimed in claim 35 or 41, wherein, when the drain is the ferromagnetic drain, the source is a non-magnetic source that comprises a non-magnetic tunnel barrier joined to the ferromagnetic semiconductor layer, and a non-magnetic electrode joined to the non-magnetic tunnel barrier.

44. The transistor as claimed in claim 35, wherein the source and the drain are a ferromagnetic

source and a ferromagnetic drain each comprising a ferromagnetic tunnel barrier joined to the ferromagnetic semiconductor layer, and a non-magnetic electrode joined to the ferromagnetic tunnel barrier.

45. The transistor as claimed in any of claims 35 to 44, wherein:

an energy barrier due to the ferromagnetic tunnel barrier or the non-magnetic tunnel barrier is formed at least on the side of the conduction band, when the carriers are electrons; and

the energy barrier is formed at least on the side of the valence band, when the carriers are holes.

46. The transistor as claimed in any of claims 35 to 45, wherein the ferromagnetic semiconductor layer is formed with a ferromagnetic semiconductor having magnetic elements added to a semiconductor.

47. The transistor as claimed in any of claims 35 to 46, wherein the ferromagnetic source or the ferromagnetic drain comprises the ferromagnetic electrode that is a ferromagnetic metal, a ferromagnetic semiconductor, or a half-metal ferromagnetic material.

48. The transistor as claimed in any of claims 35 to 46, wherein:

the ferromagnetic source or the ferromagnetic drain includes an insulating ferromagnetic material as the ferromagnetic tunnel barrier;

at least the band edge of the conduction band of the insulating ferromagnetic material is spin-split, when the carriers are electrons; and

at least the band edge of the valence band of the insulating ferromagnetic material is spin-split, when the carriers are holes.

49. The transistor as claimed in any of claims 35 to 48, wherein the ferromagnetic semiconductor employed for the ferromagnetic electrode is a ferromagnetic semiconductor having magnetic elements added to a semiconductor.

50. The transistor as claimed in any of claims 35 to 47, wherein, when the ferromagnetic electrode is a half-metal ferromagnetic material, the non-magnetic tunnel barrier or the ferromagnetic tunnel barrier forms an energy barrier in relation to the metallic spin band of the half-metal ferromagnetic material.

51. The transistor as claimed in any of claims 35 to 50, wherein an insulating layer is interposed between the gate electrode and the ferromagnetic semiconductor layer.

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52. The transistor as claimed in claim 51, wherein the insulating layer comprises a surface oxide layer that is formed by oxidizing the surface of the ferromagnetic semiconductor layer.

53. The transistor as claimed in claim 51, wherein the insulating layer is grown or deposited on the ferromagnetic semiconductor layer.

54. The transistor as claimed in any of claims 35 to 53, wherein the transistor is formed on a substrate made of a semiconductor, a substrate having a semiconductor layer formed thereon, or a substrate having an insulating layer formed thereon.

55. The transistor as claimed in claim 54, wherein:

the transistor is formed on the substrate;

the junction interface of the source and the drain in the vicinity of the gate electrode is substantially perpendicular to the principal surface of the substrate; and

the flowing direction of the carriers moving from the source to the drain is in a plane substantially parallel to the principal surface of the substrate.

56. The transistor as claimed in claim 54 or 55, wherein the ferromagnetic electrode or the non-magnetic electrode is separated from the ferromagnetic semiconductor layer and the substrate by the non-magnetic tunnel barrier or the ferromagnetic tunnel barrier.

57. The transistor as claimed in claim 54, wherein:

the transistor is formed on the substrate;

the junction interface of the source and the drain with the ferromagnetic semiconductor is substantially parallel to the principal surface of the substrate; and

the flowing direction of the carriers moving from the source to the drain is substantially perpendicular to the principal surface of the substrate.

58. The transistor as claimed in claim 54 or 57, comprising:

a stacked structure in which the source, the ferromagnetic semiconductor, and the drain are stacked substantially in parallel with the principal surface of the substrate; and

a gate insulating film and a gate electrode that are formed on a side surface of the stacked structure.

59. The transistor as claimed in claim 58, wherein a conductive semiconductor layer formed on the

substrate serves as a contact layer for the source.

60. Transistors as claimed in claim 58, wherein a conductive semiconductor layer formed on the substrate serves as a common contact layer for the sources of the transistors.

61. The transistor as claimed in claim 54, wherein:

the transistor is formed on the substrate;

the junction interface of the source and the drain with the ferromagnetic semiconductor in the vicinity of the gate electrode is substantially parallel to the principal surface of the substrate; and

the flowing direction of the carriers moving from the source to the drain is in a plane substantially parallel to the principal surface of the substrate.

62. The transistor as claimed in claim 61, wherein:

a structure in which a ferromagnetic semiconductor layer, a non-magnetic tunnel barrier, and a ferromagnetic electrode are stacked in this order, or a structure in which a ferromagnetic semiconductor layer, a ferromagnetic tunnel barrier, and a non-magnetic electrode are stacked in this order is formed on the substrate;

a concave portion is formed in the substrate, the concave portion having a bottom with such a depth as to reach the ferromagnetic semiconductor layer or the inside of the ferromagnetic magnetic semiconductor layer; and

a gate insulating film and a gate electrode are formed on the inner surface of the concave portion.

63. The transistor as claimed in any of claims 35 to 62, wherein the magnetization configuration

between the ferromagnetic semiconductor layer and the ferromagnetic electrode or the ferromagnetic tunnel barrier contained in the ferromagnetic source or the ferromagnetic drain can be adjusted to parallel magnetization or antiparallel magnetization by changing the magnetization direction of the ferromagnetic semiconductor layer.

64. The transistor as claimed in any of claims 54 to 62, wherein the magnetization configuration between the ferromagnetic semiconductor layer and the ferromagnetic electrode or the ferromagnetic tunnel barrier contained in the ferromagnetic source and the ferromagnetic drain can be adjusted to parallel magnetization or antiparallel magnetization by changing the magnetization direction of the ferromagnetic semiconductor layer, with the magnetization configuration between the ferromagnetic materials contained in the ferromagnetic source and the ferromagnetic drain being fixed to parallel magnetization.

65. The transistor as claimed in any of claims 35 to 62, wherein the magnetization configuration between the ferromagnetic semiconductor layer and the ferromagnetic electrode or the ferromagnetic tunnel barrier contained in the ferromagnetic source or the ferromagnetic drain can be adjusted to parallel magnetization or antiparallel magnetization by changing the magnetization direction of the ferromagnetic electrode or the ferromagnetic tunnel barrier contained in the ferromagnetic source or the ferromagnetic drain.

66. The transistor as claimed in any of claims 54 to 62, wherein the magnetization configuration between the ferromagnetic semiconductor layer and the ferromagnetic electrode or the ferromagnetic tunnel

barrier contained in the ferromagnetic source and the ferromagnetic drain can be adjusted to parallel magnetization or antiparallel magnetization by changing the magnetization direction of the ferromagnetic electrode or the ferromagnetic tunnel barrier contained in the ferromagnetic source and the ferromagnetic drain.

67. The transistor as claimed in any of claims 35 to 66, wherein the injection of the carriers from the source to the ferromagnetic semiconductor layer is restricted by the ferromagnetic tunnel barrier or the non-magnetic tunnel barrier in the junction of the ferromagnetic semiconductor layer with the ferromagnetic source or the non-magnetic source, while a voltage is not applied between the gate electrode and the ferromagnetic source or the non-magnetic source.

68. The transistor as claimed in any of claims 35 to 67, wherein the carriers tunnel the ferromagnetic tunnel barrier or the non-magnetic tunnel barrier, and are injected into the ferromagnetic semiconductor layer, upon application of a voltage between the gate electrode and the ferromagnetic source or the non-magnetic source.

69. The transistor as claimed in any of claims 35 to 68, wherein, when the magnetization configuration of the ferromagnetic semiconductor layer with respect to the ferromagnetic source or the ferromagnetic drain, or to the ferromagnetic source and the ferromagnetic drain, is parallel magnetization, a drain current is lower than a drain current generated in a case where the magnetization configuration is antiparallel magnetization.

70. The transistor as claimed in any of claims 35 to 69, wherein trans conductance can be controlled

in accordance with the relative magnetization direction of the ferromagnetic semiconductor layer with respect to the ferromagnetic source or the ferromagnetic drain, or to the ferromagnetic source and the ferromagnetic drain, with the same bias being applied.

71. The transistor as claimed in any of claims 35 to 70, wherein, when the magnetization configuration of the ferromagnetic semiconductor layer with respect to the ferromagnetic source or the ferromagnetic drain, or to the ferromagnetic source and the ferromagnetic drain, is parallel magnetization, a threshold voltage is set as a gate voltage for generating a predetermined current between the ferromagnetic source and the ferromagnetic drain by applying a current to the gate electrode.

72. The transistor as claimed in any of claims 35 to 71, wherein:

the transistor stores information in accordance with the relative magnetization direction of the ferromagnetic semiconductor layer with respect to the ferromagnetic source or the ferromagnetic drain, or to the ferromagnetic source and the ferromagnetic drain; and

the transistor detects information stored in the transistor, based on the trans conductance of the transistor that depends on the relative magnetization direction of the ferromagnetic semiconductor layer with respect to the ferromagnetic source or the ferromagnetic drain, or to the ferromagnetic source and the ferromagnetic drain.

73. The transistor as claimed in claim 72, wherein the transistor rewrites information by applying such a bias to the source and the drain that the ferromagnetic semiconductor layer exhibits

paramagnetism, applying a magnetic field to the ferromagnetic semiconductor layer so as to change the magnetization direction of the ferromagnetic semiconductor layer in the paramagnetic state, and then cutting off the application of the bias to the source and the drain while the application of the magnetic field is continued or applying such a bias as to return the ferromagnetic semiconductor layer to a ferromagnetic state.

74. The transistor as claimed in claim 72, wherein the transistor rewrites information by applying such a bias to the source and the drain as to put the ferromagnetic semiconductor layer into a ferromagnetic state with sufficiently small coercive force, applying a magnetic field to the ferromagnetic semiconductor layer so as to change magnetization direction of the ferromagnetic semiconductor layer in the ferromagnetic state with the sufficiently coercive force, and then cutting off the application of the bias to the source and the drain while the application of the magnetic field is continued or applying such a bias as to return the ferromagnetic semiconductor layer to the original ferromagnetic state with greater coercive force.

75. The transistor as claimed in claim 72, wherein the transistor rewrites information by applying a bias to the source and the drain so as to demagnetize the ferromagnetic semiconductor layer, and then applying a magnetic field to the ferromagnetic semiconductor layer to utilize the initial magnetization configuration.

76. The transistor as claimed in claim 72, wherein the transistor reads out information based on a current flowing between the drain and the gate electrode, when a predetermined voltage is applied to

the drain and the gate electrode, with the source being the reference.

77. A memory element comprising:

the transistor as claimed in any of claims 35 to 76;

a first line that is connected to the gate electrode;

a second line that is connected to the drain; and

a third line that grounds the source.

78. The memory element as claimed in claim 77, comprising

an information rewrite unit that rewrites information by applying a first voltage to the second line and the third line so that the ferromagnetic semiconductor layer changes from a ferromagnetic state with large coercive force to a paramagnetic state, applying a current to the first line to induce such a magnetic field as to change the magnetization direction of the ferromagnetic semiconductor layer, and then cutting off the application of the first voltage or applying a second voltage so as to return the ferromagnetic semiconductor layer to the ferromagnetic state.

79. The memory element as claimed in claim 77, comprising

an information rewrite unit that rewrites information by applying a first voltage to the second line and the third line so that the ferromagnetic semiconductor layer changes from a ferromagnetic state with large coercive force to a ferromagnetic state with sufficiently small coercive force, applying a current to the first line to induce such a magnetic field as to change the magnetization direction of the ferromagnetic semiconductor layer, and then cutting off the

application of the first voltage or applying a second voltage so as to return the ferromagnetic semiconductor layer to the ferromagnetic state with the large coercive force.

80. The memory element as claimed in claim 77, comprising

an information rewrite unit that rewrites information by applying a first voltage to the second line and the third line so that the ferromagnetic semiconductor layer is put into to a demagnetized state, and applying a current to the first line to induce such a magnetic field as to magnetize the ferromagnetic semiconductor layer utilizing initial magnetization characteristics after the application of the first voltage is cut off.

81. The memory element as claimed in claim 77, wherein the memory element reads out information, based on a current flowing between the second line and the third line, when predetermined voltages are applied to the second line and the first line, with the third line being the reference.

82. A memory circuit comprising:

transistors as claimed in any of claims 35 to 76;

a ground line that collectively grounds the sources of a first group of transistors that are selected from the transistors;

a word line that are collectively connected to the gates of the first group of transistors; and

a bit line that are connected to the drains of the first group of transistors independently of one another, and are also collectively connected to a second group of transistors including transistors that do not belong to the first group.

83. A memory circuit comprising:

transistors as claimed in any of claims 35 to 76;

a ground line that is collectively connected to the sources of transistor that belong to a transistor column comprising the transistors, the transistors belonging to the transistor column being aligned in one direction;

a word line that is collectively connected to the gates of the transistors that belong to the transistor column; and

bit lines that are connected to the drains of the transistors in the transistor column independently of one another.

84. A memory circuit comprising:

transistors as claimed in any of claims 35 to 76, the transistors being arranged in a matrix fashion;

ground lines that are collectively connected to the sources of the transistors aligned in a column direction;

word lines that are collectively connected to the gate electrodes of the transistors aligned in the column direction; and

bit lines that are collectively connected to the drains of the transistors aligned in a row direction.

85. A memory circuit comprising:

a first transistor and a second transistor as claimed in any of claims 35 to 76, the first and second transistors being adjacent to each other;

a word line that is respectively connected to the gate electrode of the first transistor and the gate electrode of the second transistor;

a first bit line that is connected to the drain of the first transistor;

a second bit line that is connected to the drain of the second transistor;

a source that is shared between the first and second transistors; and

a line that grounds the shared source, and extends in a direction perpendicular to the bit lines.

86. The memory circuit as claimed in any of claims 83 to 85, comprising

an information rewrite unit that rewrites information stored in a transistor selected through the word line and the bit line, the rewrite being performed by applying a first voltage to the bit line and the ground line so that the ferromagnetic semiconductor layer changes from a ferromagnetic state to a paramagnetic state, applying a current to the word line to induce such a magnetic field as to change the magnetization direction of the ferromagnetic semiconductor layer, and then cutting off the application of the first voltage or applying a second voltage so as to return the ferromagnetic semiconductor layer to the ferromagnetic state.

87. The memory element or the memory circuit as claimed in any of claims 82 to 85, comprising

an information rewrite unit that rewrites information stored in a transistor selected through the word line and the bit line, the rewrite being performed by applying a first voltage to the bit line and the ground line so that the ferromagnetic semiconductor layer changes from a ferromagnetic state with large coercive force to a ferromagnetic state with sufficiently small coercive force, applying a current to the word line to induce such a magnetic field as to change the magnetization direction of the ferromagnetic semiconductor layer, and then cutting off the application of the first voltage or applying a second voltage so as to return the ferromagnetic semiconductor layer to the ferromagnetic state.

88. The memory circuit as claimed in any of claims 83 to 85, comprising

an information rewrite unit that rewrites information by applying a first voltage to the bit line and the ground line so that the ferromagnetic semiconductor layer is put into to a demagnetized state, applying a current to the word line to induce such a magnetic field as to magnetize the ferromagnetic semiconductor layer, and utilizing initial magnetization characteristics after the application of the first voltage is cut off.

89. The memory circuit as claimed in any of claims 82 to 85, wherein the memory circuit reads out information stored in a transistor selected through the word line and the bit line, based on the intensity of a current flowing between the word line and the ground line, when predetermined voltages are applied to the bit line and the word line, with the ground line being the reference.

90. A memory circuit comprising:

transistors as claimed in any of claims 35 to 76;

a ground line that collectively grounds the sources of a first group of transistors that are selected from the transistors;

a bit line that are collectively connected to the drains of the first group of transistors; and

a word line that are connected to the gates of the first group of transistors independently of one another, and are also collectively connected to a second group of transistors including transistors that do not belong to the first group.

91. A memory circuit comprising:

transistors as claimed in any of claims 35 to 76;

a ground line that is collectively connected to the sources of transistor that belong to a transistor row comprising the transistors, the transistors belonging to the transistor row being aligned in one direction;

a bit line that is collectively connected to the drains of the transistors that belong to the transistor row; and

word lines that are connected to the gates of the transistors in the transistor row independently of one another.

92. A memory circuit comprising:

transistors as claimed in any of claims 35 to 76, the transistors being arranged in a matrix fashion;

ground lines that are collectively connected to the sources of the transistors aligned in a row direction;

word lines that are respectively connected to the gate electrodes of the transistors aligned in a column direction; and

bit lines that are collectively connected to the drains of the transistors aligned in the row direction.

93. A memory circuit comprising:

transistors as claimed in any of claims 35 to 76, the transistors being arranged in a matrix fashion;

ground lines that are collectively connected to the sources of the transistors aligned in a row direction;

word lines that are collectively connected to the gate electrodes of the transistors aligned in a column direction; and

bit lines that are collectively connected to the drains of the transistors aligned in the row direction,

ground lines adjacent to each other in the column direction being formed by one line among the ground

lines.

94. A memory circuit comprising:

a first transistor and a second transistor as claimed in any of claims 35 to 76, the first and second transistors being adjacent to each other;

a word line that is collectively connected to the gate electrode of the first transistor and the gate electrode of the second transistor;

a first bit line that is connected to the drain of the first transistor;

a second bit line that is connected to the drain of the second transistor;

a source that is shared between the first and second transistors; and

a line that grounds the shared source, and extends in a direction parallel to the bit lines.

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95. The memory circuit as claimed in any of claims 90 to 94, comprising

an information rewrite unit that collectively rewrites information stored in the transistors that are connected to the bit line and the ground line and are also connected to the word lines to which a current is applied, the rewrite being performed by applying a first voltage to the bit line and the ground line so that the ferromagnetic semiconductor layer changes from a ferromagnetic state with large coercive force to a paramagnetic state, applying the current simultaneously to the word lines to induce such a magnetic field as to change the magnetization direction of the ferromagnetic semiconductor layer, and then cutting off the application of the first voltage or applying a second voltage so as to return the ferromagnetic semiconductor layer to the ferromagnetic state.

96. The memory circuit as claimed in any of

claims 90 to 94, comprising

an information rewrite unit that collectively rewrites information stored in the transistors that are connected to the bit line and the ground line and are also connected to the word lines to which a current is applied, the rewrite being performed by applying a first voltage to the bit line and the ground line so that the ferromagnetic semiconductor layer changes from a ferromagnetic state with large coercive force to a ferromagnetic state with sufficiently small coercive force, applying the current simultaneously to the word lines to induce such a magnetic field as to change the magnetization direction of the ferromagnetic semiconductor layer, and then cutting off the application of the first voltage or applying a second voltage so as to return the ferromagnetic semiconductor layer to the ferromagnetic state.

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97. The memory circuit as claimed in any of claims 90 to 94, comprising

an information rewrite unit that rewrites information by applying a first voltage to the bit line and the ground line so that the ferromagnetic semiconductor layer is put into to a demagnetized state, and applying a current to the word lines to induce such a magnetic field as to magnetize the ferromagnetic semiconductor layer utilizing initial magnetization characteristics after the application of the first voltage is cut off.

98. The memory circuit as claimed in any of claims 90 to 93, wherein the memory circuit reads out information stored in a transistor selected through the word line and the bit line, based on the size of a current flowing between the word line and the ground line, when predetermined voltages are applied to the bit line and the word line, with the ground line being

the reference.

99. The memory element or the memory circuit as claimed in any of claims 77 to 98, further comprising a yoke that surrounds the outer periphery of the word line or the first line.